WAYNE E. AMACHER
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SPECIAL QUALIFICATIONS

Have broad, in-depth knowledge of North American and international telephone systems. My key expertise is telephony design and embedded system design, initial concept to manufacturing release.

Experience with program and project management, contracts, ISO 9001, standards, specifications, schedules, document control, proposals, and international customers. I am an excellent writer. I can do anything and am always ready to try new things!

I have an MSEE and many years of experience as an electrical design engineer.

Experience Summary

- Hardware system architecture, including circuit design, parts selection, cooling design, power requirements, interface design, cable design, and packaging
- Wrote the company standards for PCB design and layout, including rules for minimizing EMI
- Wrote many detailed design specifications to guide PCB and product design
- Worked closely with marketing and top management, turning marketing requirements into hardware
- Performed liaison between marketing and hardware engineeering
- High-speed digital and analog design, PLL design
- Embedded system design using IBM Power PC, PPC440 and family, Freescale MPC8541, MSC810x DSPs; Atmel ATMEGA32L, Infineon INCA-IP and others
- Familiar with Infineon framers, Cologne ISDN chips, ADCs, Silicon Labs and Legerity SLICs, DAAs, protection circuitry, codecs, and line transformers
- Performed FPGA and CPLD design
- Experience with flash memory, hard disks, EEPROM, DDR,
- Telephony design including channel banks, media exchanges, T1/E1/J1, FXO, FXS, BRI-ST, PRI, VoIP, HDLC, phones, wireless, Bluetooth, battery, battery backup supplies, and ringing generators
- μP buses: I^2C, SPI, PCI, EIA-232, Ethernet, local and parallel buses, SCSI, and others
- Multi-layer high-speed backplanes using terminated BLVDS and GTLP, incorporating hot plug-in
- Determined bus timing and corresponding μP and peripheral device register settings for many products
- Experienced with OrCad and PROTEL. Experienced with View logic as well. Have used PADS and Allegro viewers
- Experienced with safety, EMC, and ESD control, UL60950 and international equivalents, CISPR 22/EN55022, the EN61000 series, FCC Part 68 (TIA-968), etc.
- Very familiar with the ITU-T standards, ANSI standards, Telecordia Standards, and many others
- Wireless design using Bluetooth and WI-FI (802.11b)
- Microsoft 2000, Microsoft XP, Microsoft Office, consider myself a WORD expert
- Stratum 1, 2, and 3 telephony timing systems

PROFESSIONAL EXPERIENCE

Sr. Hardware Engineer – Zultys Technologies (www.zultys.com) - 12/01 – present:

I was one of the founders of Zultys in 2001. Defined and specified the hardware architecture for almost all Zultys products. Worked closely with marketing to write the hardware specifications for each product and for each PCB assembly: MX1200. MX250, MX25, MX30 MX30P, BPS12, BPS2, ZIP4X4, WIP2 and all plug-in cards. Selected processors and chip sets. Architected CPLDs and FPGAs. Made product and hardware architecturural presentations to top management and obtained the approval from top management for almost all products. Architected the buses. Specified peripheral devices including memories and memory interfaces.

Specified bus timing requirements, then defined processor register settings and peripheral device register settings to achieve timing requirements. Provided written requirements to the firmware group (firmware relied on my specifications to design the hardware interfaces). Calculated power requirements. Calculated and specified heat dissipation, cooling requirements, heat sinks, and fans. Designed cables and interconnections. Selected hard disks. Specified all electrical interfaces. Specified the physical architecture of each unit. Ensured that all products were designed to meet worldwide safety and EMC requirements. Am very familiar with almost all international standards affecting telephony, safety, and EMC. Designed PCBs using OrCad. I mostly wrote hardware design specifications and designed a few boards; I am intimately familiar with and fully understand every schematic at Zultys

Served as the EMC and safety engineer in the beginning.

Zultys laid everyone off while they sought additional funding, but remained operational. During that time I worked part-time as a volunteer at Zultys assisting marketing during the funding search. When Zultys entered Chapter 11 Bankruptcy, they hired me back until the company was sold in November 2006. I wrote the first 11 entries concerning customer successes at http://www.zultys.com/index.jsp?tab=customer_successes.

Group Leader – Zarak Systems Division of Spirent Communications - 3/98 – 8/01:

Served as the hardware system architect for the Abacus2 system, "a city's worth of calls". The Abacus2 performs bulk call generation and switching for testing telecom equipment. Was responsible for all aspects of the hardware design, PCBs (System Controller, T1/E1, T3/E3.G.747, link to Abacus1, analog subscriber line interfaces, etc), hardware interfaces to software, packaging, EMC, safety, connectorization, mechanical design, high-speed backplane and hot insertion. The 17 inch backplane runs synchronously at 16.384 MHz. The backplane, including hot insertion, worked the first time! The backplane has the maximum capability of handling up to 28,272+ channels, each of which can be switched to any other channel, non-blocking. Abacus2's maximum capacities are 16-T3s, 16-E3s, 448-T1s, 320-E1s, 1200-analog circuits.

PROJECT ENGINEER – VISTA LABS - 9/97 – 3/98

Design of stratum 1 and lower timing systems for T1 and E1 telephone offices. Started off designing two boards, the Synchronization Monitor and the Alarm board, ended up successfully managing the entire project including 6 hardware and software engineers plus technicians and several consultants to a very tight schedule. The synchronization monitor board measures phase shift to 0.5 nanosecond resolution. It outputs TIE, MTIE, jitter, and wander. Learned TL1. System required hot plug-in and used direct digital frequency synthesis (DDFS) for clock generation.

SENIOR DESIGN ENGINEER – OPTICAL MICROWAVE NETWORKS, INC. - 11/94 – 9/97

Telephony, data, modem, FPGA and PCB experience. Designed E1 drop and insert channel bank, charge pump ringing generator, line cards, data interfaces, phase-locked-loops, converted high speed satellite data packets to data rate, designed world-wide modem I/F. Used Orcad for PCB design and View logic for FPGA design and simulation. Used MicroSim (Pspice) for analog simulation. Responsible for ISO 9001 compliance.

CONTRACT ENGINEER – T-COM CORPORATION - 12/92 – 10/94

As Project Engineer designed a multi-channel, combination DCE/DTE data interface for T-COM's primary T1 test instrument. Converted all data rates: Subrates (2.4 - 38.4Kbs), Switched 56, 64Kbs Clear Channel, and FT1 (56Kbs -1.536Mbs) from/to DS0-A, DS0-B, and T1. Included ESF data link and secondary channels. Data interfaces were RS-232 and V.35. The project included three circuit boards, an embedded microprocessor, six Xilinx FPGAs, phase-locked Loops (PLLs) as well as HCMOS logic. Used OrCAD and XACT CAE schematic capture and programming software. Filled in as Engineering Manager while VP of Engineering was on sabbatical.

CONTRACT ENGINEER – DIABLO RESEARCH. - 9/92 – 12/92

Worked on the engineering design of an RF excited electronic light bulb. Concerned with packaging, UL approval, and high Q ceramic capacitors.

PROJECT MANAGER/CONTRACT ENGINEER – COMPUTER AIDED SERVICE. - 9/90 – 5/92

Managed the development from prototype to production of state-of- the-art, PC based, diagnostic equipment for the automotive test market in a privately held start-up. Responsibilities included planning, scheduling, hardware design, test, EMI, introduction into manufacturing, cost reduction, and change control.

PROJECT ENGINEER – LITTON APPLIED TECHNOLOGY - 1980 – 1990

As Project Engineer, successfully architected, designed, and managed the development of a $26M, VDE compliant, state-of-the- art, radar simulator for the German Tornado Aircraft Flight Trainer from concept to last shipment. It included fourteen new printed circuit designs. It met all requirements including on-schedule acceptance by the customer. Was the responsible engineer for VDE compliance. Reliability was outstanding - virtually no failures. Made 25% profit.

As Program Manager managed an update of the same System. Responsible for contract, statement of work, documentation, deliverables, schedule, cost, and functional compliance. Met all requirements, with on schedule delivery and acceptance. Made 25% profit. Customer very satisfied with both programs.

Served as Assistant Project Manager of a state-of-the-art, MIL-SPEC, $24M, airborne radar warning system for a foreign customer. Responsible for program planning, electrical and mechanical hardware.

ENGINEERING MANAGER – LUXTRON CORPORATION - 1980

Managed the design, development, and test of a microprocessor based flouroptic temperature-sensing instrument that used optical fibers and fluorescent phosphors. The instrument had medically intrusive hyperthermia applications.

MANAGER, BUSINESS COMMUNICATIONS SYSTEMS – BNR, INC. - 1975 – 1980

Managed hardware development of a digital, multi-microprocessor PABX with digital transmission of integrated voice and data to the phone. Led both electrical and mechanical engineering. Included 40 molded plastic parts.

ELECTRICAL ENGINEERING MANAGER - PRIOR TO 1975

UNITOTE/REGITEL CORPORATION – Managed Development of Point of Sale (POS) Terminals using the 4040, 8080, and 6800 microprocessors. It used TTL-MSI "state machine" architecture and RS-232 data transmission. **GTE/IS NOVAR CORPORATION –** Designed and supervised development of IBM compatible data terminals. Designed discrete TTL CPU and its machine and assembly language. Designed the development support system. The system included masked ROM, proprietary magnetic tape transport, and packaging.
GTE SYLVANIA – Digital and analog design, signal processing, signal detection, direction finding, CRT displays, LORAN C, receivers, automatic check out equipment, ECM, Hawk Missile System, and an HF phased array antenna.

EDUCATION AND RELATED EXPERIENCE

Five college courses, UNIX, C, and C++ Programming, 9/92 - 12/93
MSEE, San Jose State University, San Jose, CA
BSEE, Case Western Reserve University, Cleveland, OH
Management seminars including Kepner-Tregoe, Transactional Analysis, Time and Program Management
Lecturer, San Jose State University: Graduate course, "The Design of Digital Systems"

PROFESSIONAL AND COMMUNITY SERVICE ACTIVITIES

Senior Member and Officer, IEEE
- Was a candidate for Director, Region 6, IEEE
- Organized and chaired many one day meetings

Past Secretary, Region 6, IEEE
- Chaired a national IEEE committee
- Planned four successful national workshops

Planned Asilomar Microcomputer Workshop Organized Micro-Mouse contest at Calif. colleges

Was chairman of the Sunnyvale School District Budget Advisory Committee for two years
Was President of Cherry Chase School PTA

Products that I architected at Zultys Won the Following Awards

Others, of course, contributed as well, but I am quite proud of my contributions.

TechWorld
2006 Product of the Year
MX30

Internet Telephony
2005 Product of the Year
WIP 2

IT Week Labs
2005 Excellence Award
MX250, ZIP Phones

SearchNetworking.com
2004 Best Product of the Year Award
ZIP 4x5

Communications Convergence
2003 Editor's Choice Award
MX1200

InfoWorld
2005 Technology of the Year Award
MX250

Network World
2003 Top 10 Startups to Watch
Zultys

Pulver 100 Companies
to Watch in 2005
Zultys

INTERNET TELEPHONY
2003 Product of the Year
MX250

China Information World
2004 Excellent Apotheosis Award
for Enterprise VoIP Applications
MX250

Communications Convergence
2003 Product of the Year
ZIP 2

Communications World Weekly
Best Product of 2003
ZIP 4x4

Communications Convergence
2004 Editor's Choice Award
MX250

TMC Labs
2003 Innovation Award
MX1200